What is claimed is:

1. A computer processor, the processor comprising:

a decode unit for decoding instruction packets fetched from a memory holding a sequence of instruction packets; and

first and second processing channels, each channel comprising a plurality of functional units, wherein the first processing channel is capable of performing control operations and comprises a control register file having a relatively narrower bit width, and the second processing channel is capable of performing data processing operations at least one input of which is a vector and comprises a data register file having a relatively wider bit width;

wherein the decode unit is operable to detect for each instruction packet whether the instruction packet defines (i) a plurality of control instructions to be executed sequentially on the first processing channel or (ii) a plurality of instructions comprising at least one data processing instruction to be executed simultaneously on the second execution channel, and to control the first and second channels in dependence on said detection.

2. A computer processor according to claim 1, wherein the first processing channel further comprises a branch unit and a control execution unit.

3. A computer processor according to claim 1, wherein the second processing channel further comprises a fixed data execution unit and a configurable data execution unit.

4. A computer processor according to claim 3, wherein the fixed data execution unit and the configurable data execution unit both operate according to a single instruction multiple data format.

5. A computer processor according to claim 1, wherein the first and second processing channels share a load store unit.

6. A computer processor according to claim 5, wherein the load store unit uses control information supplied by the first processing channel and data supplied by the second processing channel.

7. A computer processor according to claim 1, wherein the instruction packets are all of equal bit length.

8. A computer processor according to claim 7, wherein the instruction packets are all of a 64-bit length.

9. A computer processor according to claim 1, wherein the control instructions are all of a bit length between 18 and 24 bits.

10. A computer processor according to claim 9, wherein the control instructions are all of a 21-bit length.

11. A computer processor according to claim 7, wherein the nature of each instruction in an instruction packet is selected at least from a control instruction, a data instruction, and a memory access instruction.

12. A computer processor according to claim 11, wherein the bit length of each data instruction is 34 bits.

13. A computer processor according to claim 11, wherein the bit length of each memory access instruction is 28 bits.

14. A computer processor according to claim 1, wherein when the decode unit detects that the instruction packet defines three control instructions, the decode unit is operable to supply the first processing channel with the three control instructions whereby the three control instructions are executed sequentially.

15. A computer processor according to claim 1, wherein when the decode unit detects that the instruction packet defines two instructions comprising at least one data instruction, the decode unit is operable to supply the second processing channel with at least the data instruction whereby the two instructions are executed simultaneously.

16. A computer processor according to claim 1, wherein the decode unit is operable to read the values of a set of designated bits at predetermined bit locations in each instruction packet of the sequence, to determine:

a) whether the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction; and

b) where the instruction packet defines a plurality of instructions of which at least one is a data instruction, the nature of each of the two instructions selected from: a control instruction; a data instruction; and a memory access instruction.

17. A computer processor according to claim 3, wherein the configurable data execution unit is capable of executing more than two consecutive operations on the data provided by a single issued instruction before returning a result to a destination register file.

18. A method of operating a computer processor which comprises first and second processing channels each comprising a plurality of functional units, wherein the first processing channel comprises a control register file having a relatively narrower bit width and the second processing channel comprises a data register file having a relatively wider bit width, the method comprising:

decoding an instruction packet to detect whether the instruction packet defines a plurality of control instructions of equal length or two instructions comprising at least one data instruction, at least one of which is a vector;

when the instruction packet defines a plurality of control instructions of equal length, supplying the control instructions to the first processing channel whereby the control instructions are executed sequentially; and

when the instruction packet defines a plurality of instructions comprising at least one data instruction, supplying at least the data instruction to the second processing channel whereby the plurality of instructions are executed simultaneously.

19. A computer program product comprising program code means which include a sequence of instruction packets,

said instruction packets including a first type of instruction packet comprising a plurality of control instructions of equal length and a second type of instruction packet comprising a plurality of instructions including at least one data instruction,

wherein the computer program product is adapted to run on a computer such that the first type of instruction packet is executed by a dedicated control processing channel, and the at least one data instruction of the second instruction packet is executed by a dedicated data processing channel, the dedicated control processing channel having a relatively narrower bit width than the dedicated data processing channel.

20. A method of operating a computer processor which comprises first and second processing channels each comprising a plurality of functional units, wherein the first processing channel comprises a control register file having a relatively narrower bit width and the second processing channel comprises a data register file having a relatively wider bit width, the method comprising:

fetching a sequence of instruction packets from a program memory, all of said instruction packets containing a set of designated bits at predetermined bit locations;

decoding each instruction packet, said decoding step including reading the values of said designated bits to determine:

a) whether the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction; and

b) where the instruction packet defines a plurality of instructions of which at least one is a data instruction, the nature of each of the two instructions selected at least from: a control instruction; a data instruction; and a memory access instruction.

21. A computer program product comprising program code means which include a sequence of instruction packets,

said instruction packets including a first type of instruction packet comprising a plurality of control instructions of substantially equal length and a second type of instruction packet comprising first and second instructions including at least one data instruction,

said instruction packets including at least one indicator bit at a designated bit location within the instruction packet, wherein the computer program product is adapted to run on a computer such that said indication bit is adapted to cooperate with a decode unit of the computer to designate whether:

a) the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction; and

b) in the case when there is a plurality of instructions comprising at least one data instruction, the nature of each of the two instructions selected from: a control instruction; a data instruction; and a memory access instruction.